30 V, Low Noise, Rail-to-Rail I/O, Low Power Operational Amplifier

Data Sheet

ADA4084-2

FEATURES

Rail-to-rail input/output
Low power: 625 µA typical
Gain bandwidth product: 15.9 MHz at A_V =100 typical
Unity-gain crossover: 9.9 MHz typical
−3 dB closed-loop bandwidth: 13.9 MHz typical at ±15 V
Low offset voltage: 100 µV maximum (SOIC)
Unity-gain stable
High slew rate: 4.6 V/µs typical
Low noise: 3.9 nV/√Hz typical at 1 kHz

APPLICATIONS

Battery-powered instrumentation
Power supply control and protection
Telecommunications
DAC output amplifier
ADC input buffer

PIN CONFIGURATIONS

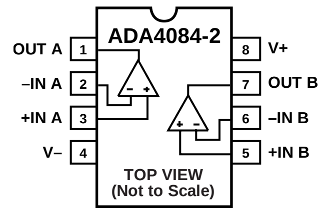

Figure 1. 8-Lead MSOP (RM)
8-Lead SOIC (R)

GENERAL DESCRIPTION

The ADA4084-2 is a dual, single-supply, 10 MHz bandwidth amplifier featuring rail-to-rail inputs and outputs. It is guaranteed to operate from 3 V to 30 V (or ±1.5 V to ±15 V).

These amplifiers are well suited for single-supply applications requiring both ac and precision dc performance. The combination of wide bandwidth, low noise, and precision makes the ADA4084-2 useful in a wide variety of applications, including filters and instrumentation.

Other applications for these amplifiers include portable telecommunications equipment, power supply control and protection, and use as amplifiers or buffers for transducers with wide output ranges. Sensors requiring a rail-to-rail input amplifier include Hall effect, piezoelectric, and resistive transducers.

The ability to swing rail-to-rail at both the input and output enables designers to build multistage filters in single-supply systems and to maintain high signal-to-noise ratios.

The ADA4084-2 is specified over the industrial temperature range of −40°C to +125°C. The dual ADA4084-2 is available in the 8-lead SOIC and MSOP surface-mount packages.

The ADA4084-2 is a member of a growing series of high voltage, low noise op amps offered by Analog Devices, Inc., (see Table 1).

For a more complete selection table of low input voltage noise amplifiers, see the AN-940 Application Note, *Low Noise Amplifier Selection Guide for Optimal Noise Performance,* available at www.analog.com.

Table 1. Low Noise Op Amps

Voltage Noise	Single	Dual	Quad
1.1 nV/Hz	AD8597	AD8599	
1.8 nV/Hz	ADA4004-1	ADA4004-2	ADA4004-4
2.8 nV/Hz RRO[1]	AD8675	AD8676	
2.8 nV/Hz	AD8671	AD8672	AD8674
3.2 nV/Hz	OP27/OP37		
3.9 nV/Hz RRIO[2]		ADA4084-2	

[1] Rail-to-rail output.
[2] Rail-to-rail input/output.

Rev. A

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REVISION HISTORY

2/12—Rev. 0 to Rev. A

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10/11—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{SY} = 3 V, V_{CM} =1.5 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage[1]	V_{OS}	SOIC package			100	µV
		−40°C ≤ T_A ≤ +125°C			200	µV
		MSOP package			130	µV
		−40°C ≤ T_A ≤ +125°C			250	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.5	1.75	µV/°C
Offset Voltage Matching		Channel A vs. Channel B, T_A = 25°C			150	µV
Input Bias Current	I_B			140	300	nA
		−40°C ≤ T_A ≤ +125°C			450	nA
Input Offset Current	I_{OS}				25	nA
		−40°C ≤ T_A ≤ +125°C			50	nA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 3 V	64	80		dB
		−40°C ≤ T_A ≤ +125°C	60			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 0.5 V ≤ V_O ≤ 2.5 V	100	104		dB
		R_L = 2 kΩ, −40°C ≤ T_A ≤ +125°C	97			dB
Input Impedance, Differential				100‖1.1		kΩ‖pF
Input Impedance, Common-Mode				80‖2.9		MΩ‖pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	2.85	2.95		V
		−40°C ≤ T_A ≤ +125°C	2.8			V
		R_L = 2 kΩ to V_{CM}	2.8	2.9		V
		−40°C ≤ T_A ≤ +125°C	2.7			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		10	20	mV
		−40°C ≤ T_A ≤ +125°C			40	mV
		R_L = 2 kΩ to V_{CM}			50	mV
		−40°C ≤ T_A ≤ +125°C			75	mV
Short-Circuit Current	I_{SC}			−17/+10		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±1.25 V to ±1.75 V	100	110		dB
		−40°C ≤ T_A ≤ +125°C	90			dB
Supply Current/Amplifier	I_{SY}	I_O = 0 mA		565	650	µA
		−40°C ≤ T_A ≤ +125°C			950	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	2.0	2.6		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 100		15.4		MHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 1		8.08		MHz
Phase Margin	Φ_M			86		Degrees
−3 dB Closed-Loop Bandwidth	−3 dB	A_V = 1, V_{IN} = 5 mV p-p		12.3		MHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.14		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		3.9		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.55		pA/√Hz

[1] Offset voltage does not include solder heat resistance.

V_{SY} = ±5.0 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage[1]	V_{OS}	SOIC package			100	µV
		−40°C ≤ T_A ≤ +125°C			250	µV
		MSOP package			130	µV
		−40°C ≤ T_A ≤ +125°C			250	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.5	1.75	µV/°C
Offset Voltage Matching		Channel A vs. Channel B, T_A = 25°C			150	µV
Input Bias Current	I_B			140	300	nA
		−40°C ≤ T_A ≤ +125°C			450	nA
Input Offset Current	I_{OS}				25	nA
		−40°C ≤ T_A ≤ +125°C			50	nA
Input Voltage Range			−5		+5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±4 V	106	124		dB
		V_{CM} = ±5 V, −40°C ≤ T_A ≤ +125°C	76			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, −4 V ≤ V_O ≤ 4 V	108	112		dB
		R_L = 2 kΩ, −40°C ≤ T_A ≤ +125°C	103			dB
Input Impedance, Differential				100‖1.1		kΩ‖pF
Input Impedance, Common-Mode				200‖2.5		MΩ‖pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	4.9	4.95		V
		−40°C ≤ T_A ≤ +125°C	4.8			V
		R_L = 2 kΩ to V_{CM}	4.8	4.85		V
		−40°C ≤ T_A ≤ +125°C	4.7			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		−4.95	−4.9	V
		−40°C ≤ T_A ≤ +125°C			−4.8	V
		R_L = 2 kΩ to V_{CM}		−4.95	−4.8	V
		−40°C ≤ T_A ≤ +125°C			−4.7	V
Short Circuit Current	I_{SC}			−24/+17		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±2 V to ±18 V	110	120		dB
		−40°C ≤ T_A ≤ +125°C	105			dB
Supply Current/Amplifier	I_{SY}	I_O = 0 mA		595	700	µA
		−40°C ≤ T_A ≤ +125°C			1000	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ to V_{CM}	2.4	3.7		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 100		15.9		MHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 1		9.6		MHz
Phase Margin	Φ_M			85		Degrees
−3 dB Closed-Loop Bandwidth	−3 dB	A_V = 1, V_{IN} = 5 mV p-p		13.9		MHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.14		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		3.9		nV/√Hz
Current Noise Density	i_n			0.55		pA/√Hz

[1] Offset Voltage does not include solder heat resistance.

V_{SY} = ±15.0 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage[1]	V_{OS}	SOIC package			100	µV
		−40°C ≤ T_A ≤ +125°C			200	µV
		MSOP package			130	µV
		−40°C ≤ T_A ≤ +125°C			250	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			0.5	1.75	µV/°C
Offset Voltage Matching		Channel A vs. Channel B, T_A = 25°C			150	µV
Input Bias Current	I_B			140	300	nA
		−40°C ≤ T_A ≤ +125°C			450	nA
Input Offset Current	I_{OS}				25	nA
		−40°C ≤ T_A ≤ +125°C			50	nA
Input Voltage Range			−15		+15	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±14 V	106	124		dB
		V_{CM} = ±15 V, −40°C ≤ T_A ≤ +125°C	85			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, −13.5 V ≤ V_O ≤ +13.5 V	110	117		dB
		−40°C ≤ T_A ≤ +125°C	105			dB
Input Impedance, Differential				100‖1.1		kΩ‖pF
Input Impedance, Common-Mode				200‖2.5		MΩ‖pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	14.8	14.9		V
		−40°C ≤ T_A ≤ +125°C	14.8			V
		R_L = 2 kΩ to V_{CM}	14.5	14.6		V
		−40°C ≤ T_A ≤ +125°C	14.3			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		−14.95	−14.9	V
		−40°C ≤ T_A ≤ +125°C			−14.8	V
		R_L = 2 kΩ to V_{CM}		−14.9	−14.8	V
		−40°C ≤ T_A ≤ +125°C			−14.7	V
Short Circuit Current	I_{SC}			±30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±2 V to ±18 V	110	120		dB
		−40°C ≤ T_A ≤ +125°C	105			dB
Supply Current/Amplifier	I_{SY}	I_O = 0 mA		625	750	µA
		−40°C ≤ T_A ≤ +125°C			1050	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	2.4	4.6		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 100		15.9		MHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 1		9.9		MHz
Phase Margin	Φ_M			86		Degrees
−3 dB Closed-Loop Bandwidth	−3 dB	A_V = 1, V_{IN} = 5 mV p-p		13.9		MHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.1		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		3.9		nV/√Hz
Current Noise Density	i_n			0.55		pA/√Hz

[1] Offset Voltage does not include solder heat resistance.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	V− ≤ V_{IN} ≤ V+
Differential Input Voltage[1]	±0.6 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

[1] For input differential voltages greater than 0.6 V, the input current should be limited to less than 5 mA to prevent degradation or destruction of the input devices.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the device soldered on a 4-layer JEDEC standard printed circuit board (PCB) with zero airflow.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC	121	43	°C/W
8-Lead MSOP	142	45	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

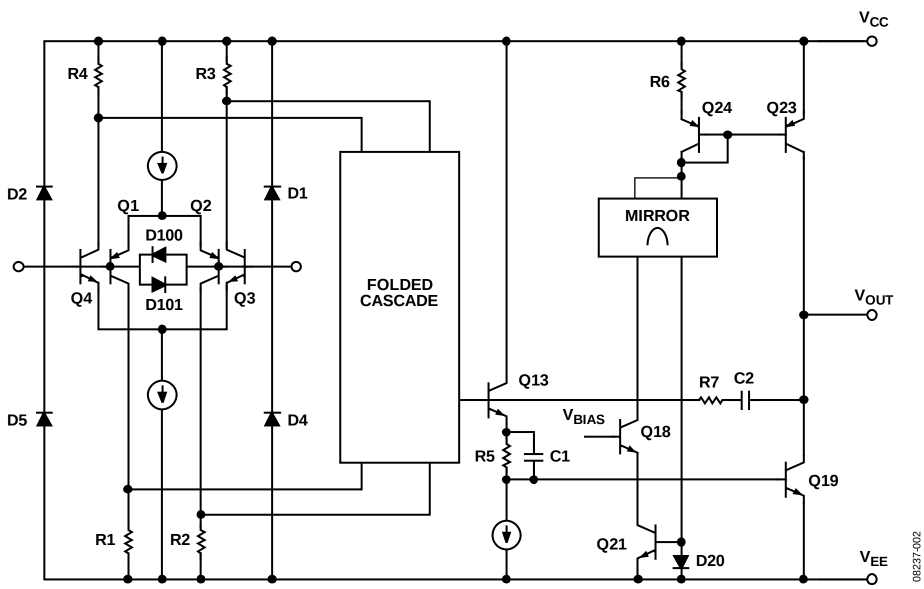

Figure 2. Simplified Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

±1.5 V CHARACTERISTICS

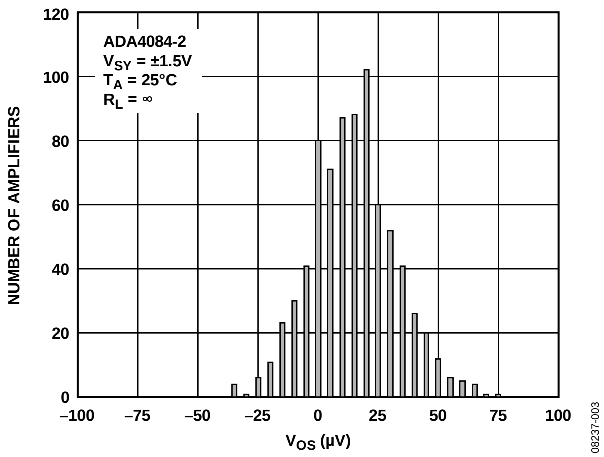

Figure 3. Input Offset Voltage Distribution, SOIC

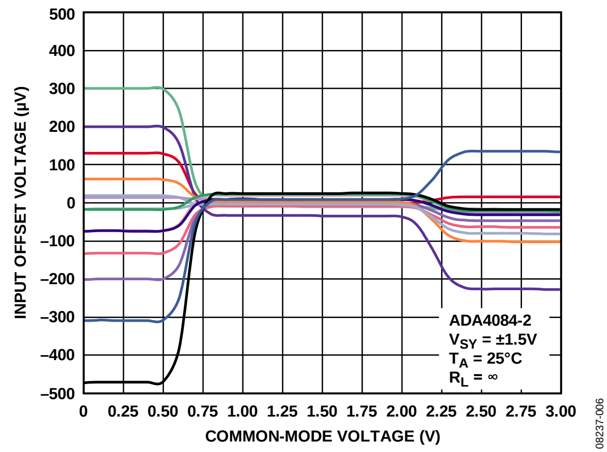

Figure 6. Input Offset Voltage vs. Common-Mode Voltage

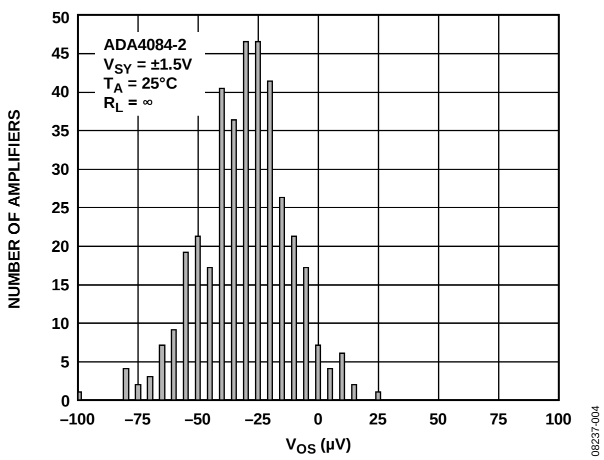

Figure 4. Input Offset Voltage Distribution, MSOP

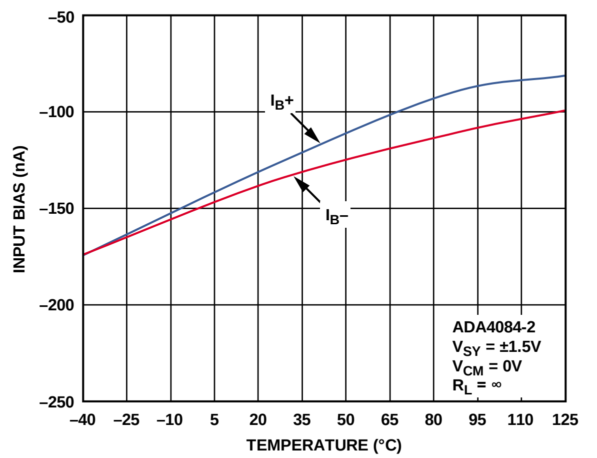

Figure 7. Input Bias Current vs. Temperature

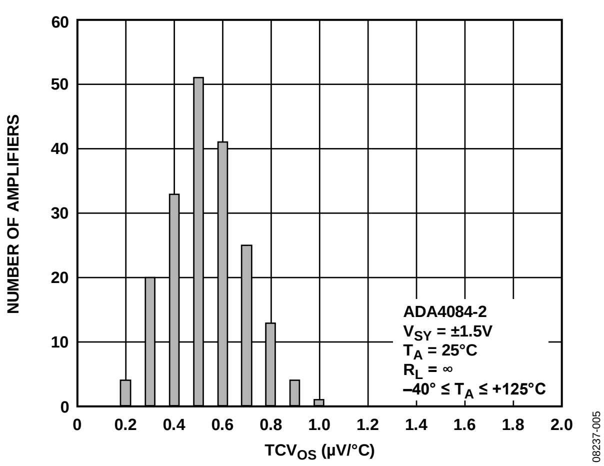

Figure 5. TCV_{OS} Distribution, SOIC

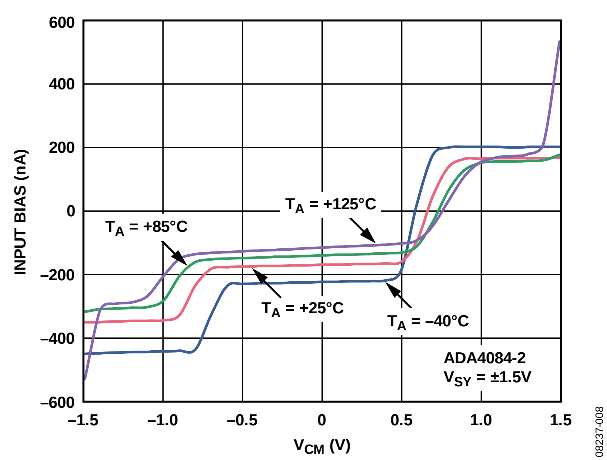

Figure 8. Input Bias Current vs. V_{CM} and Temperature

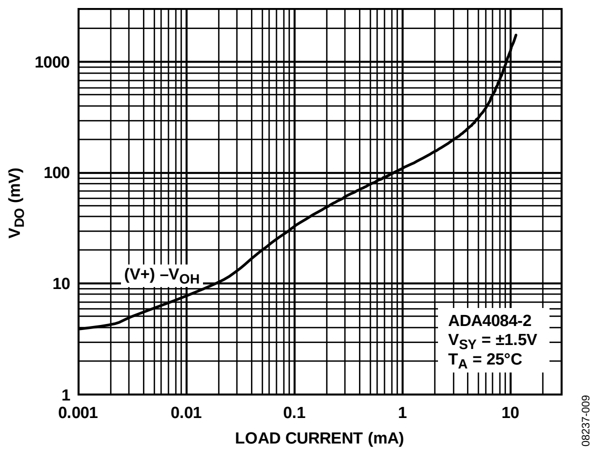

Figure 9. Dropout Voltage vs. Source Current

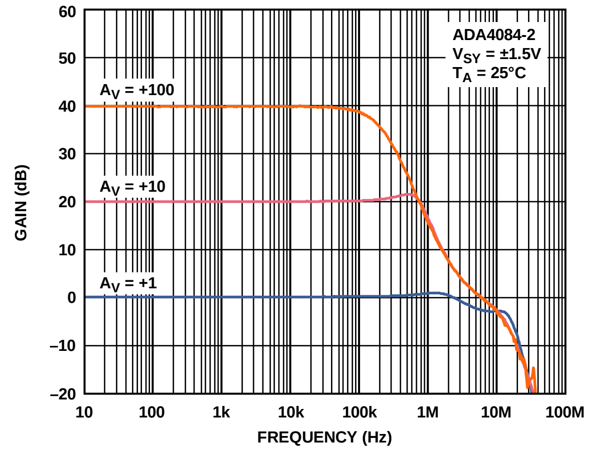

Figure 12. Closed-Loop Gain vs. Frequency

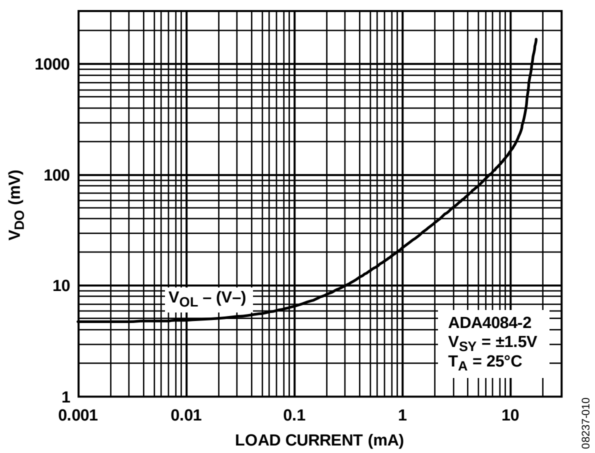

Figure 10. Dropout Voltage vs. Sink Current

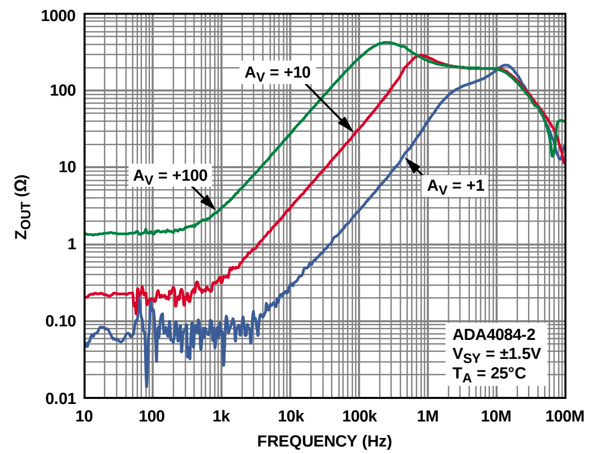

Figure 13. Output Impedance vs. Frequency

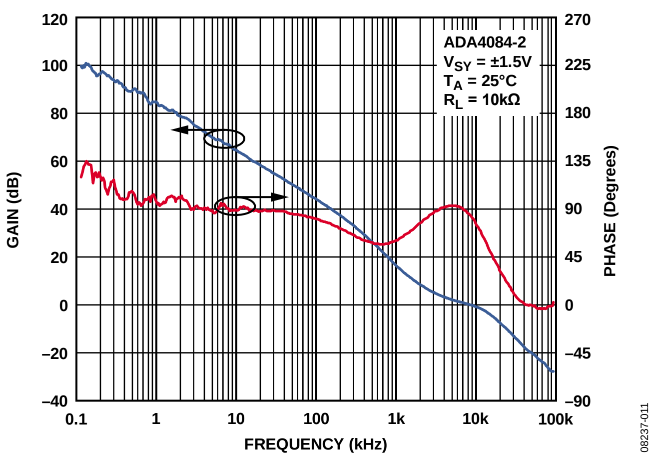

Figure 11. Open-Loop Gain and Phase vs. Frequency

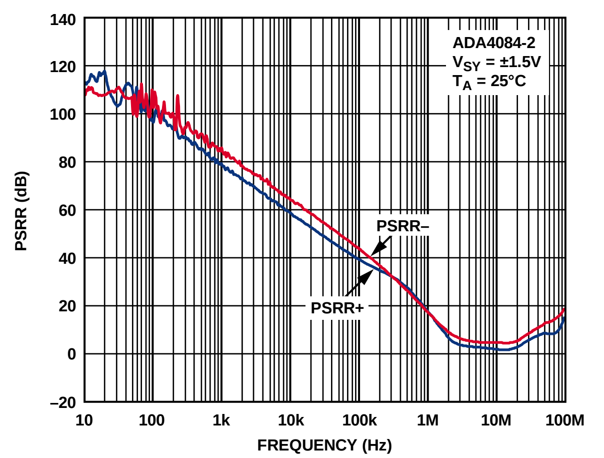

Figure 14. PSRR vs. Frequency

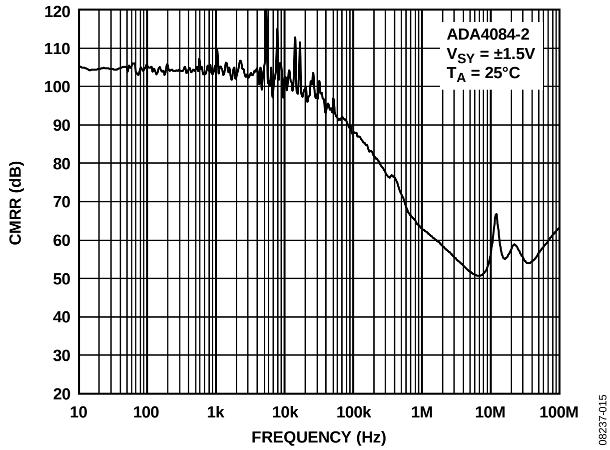

Figure 15. CMRR vs. Frequency

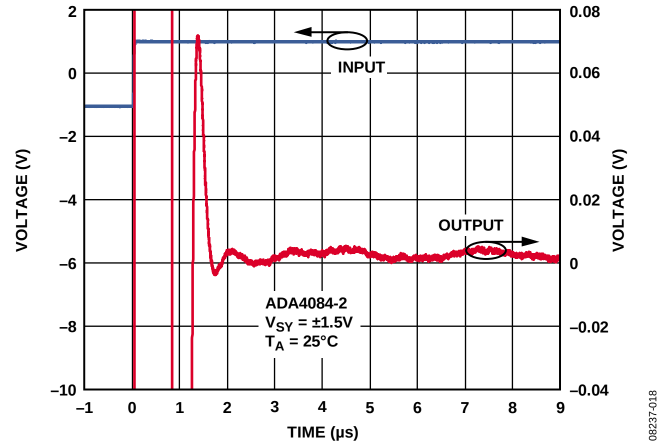

Figure 18. Settling Time

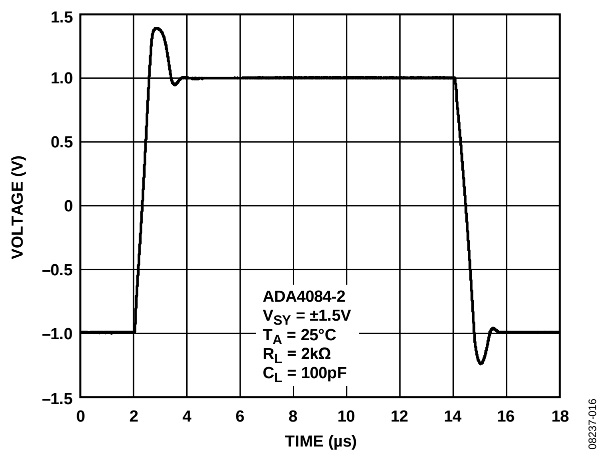

Figure 16. Large Signal Transient Response

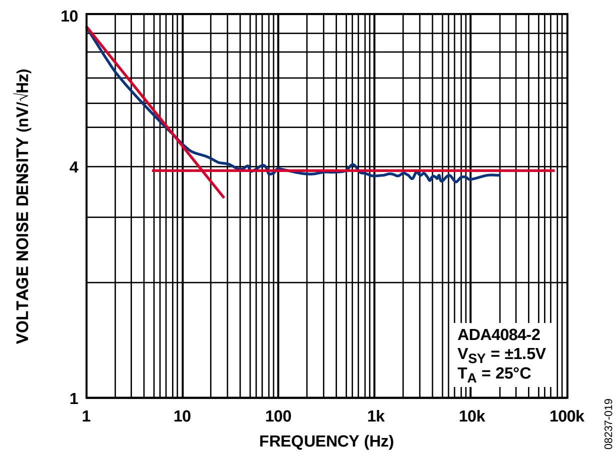

Figure 19. Voltage Noise Density

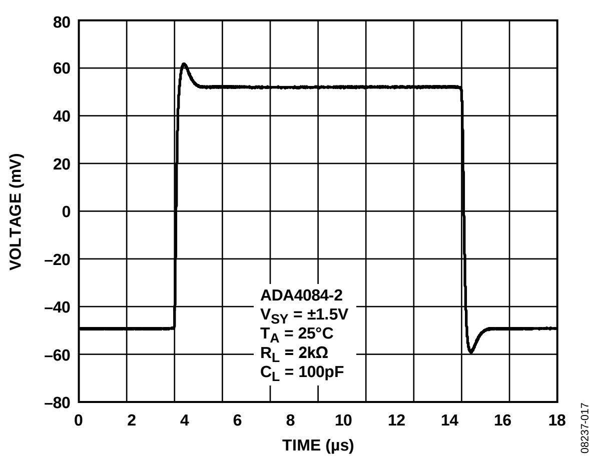

Figure 17. Small Signal Transient Response

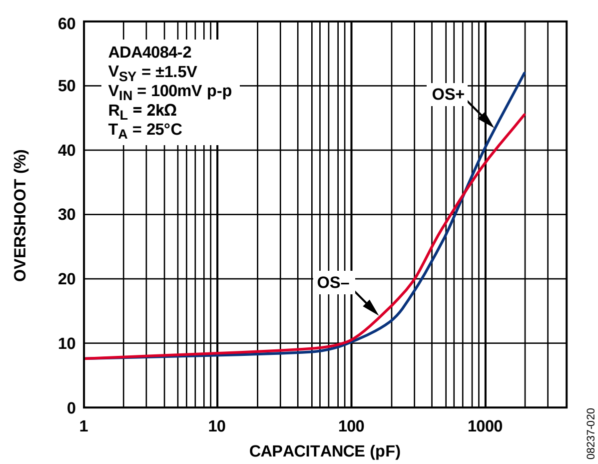

Figure 20. Overshoot vs. Capacitance

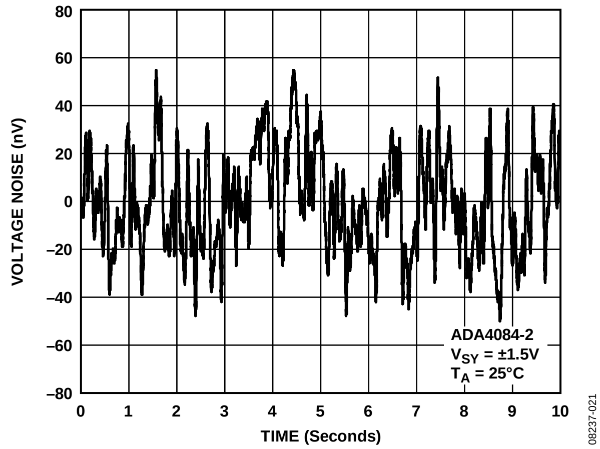

Figure 21. Voltage Noise 0.1 Hz to 10 Hz

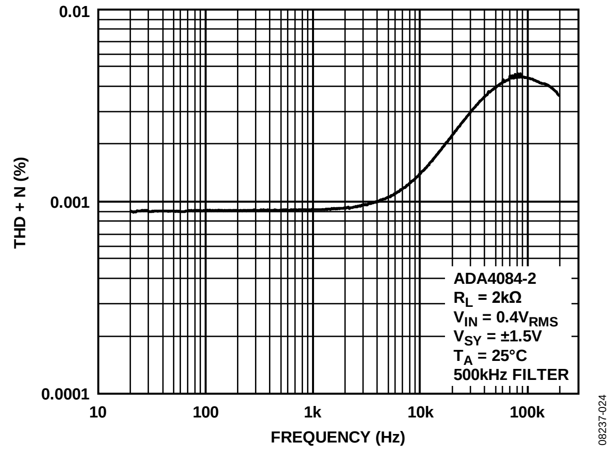

Figure 24. THD + N vs. Frequency

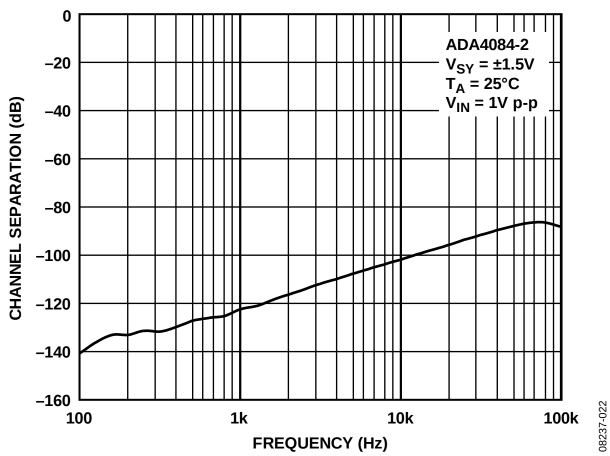

Figure 22. Channel Separation

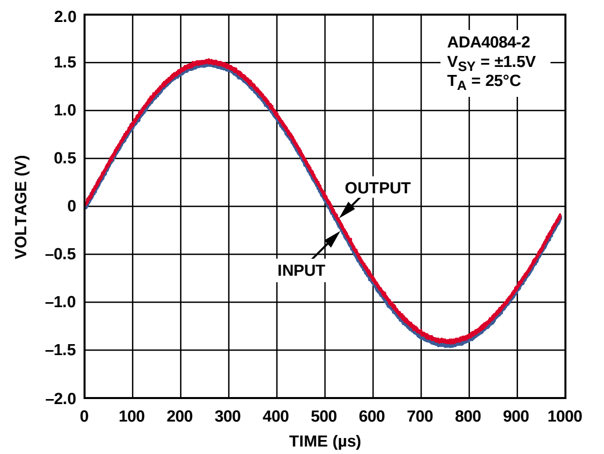

Figure 25. No Phase Reversal

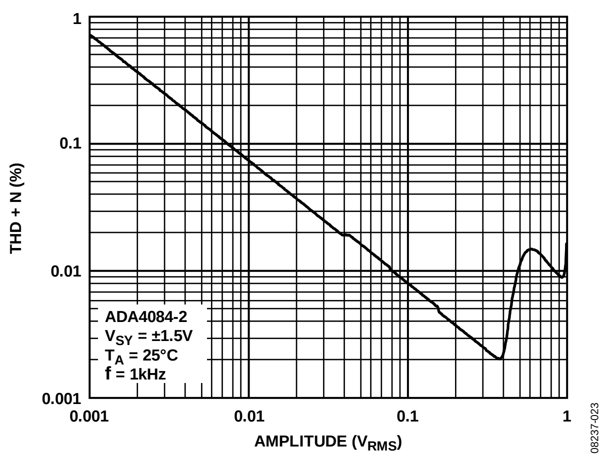

Figure 23. THD + N vs. Amplitude

±5 V CHARACTERISTICS

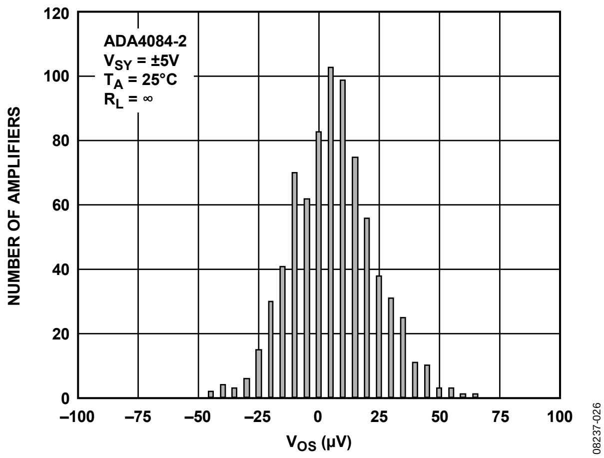

Figure 26. Input Offset Voltage Distribution SOIC

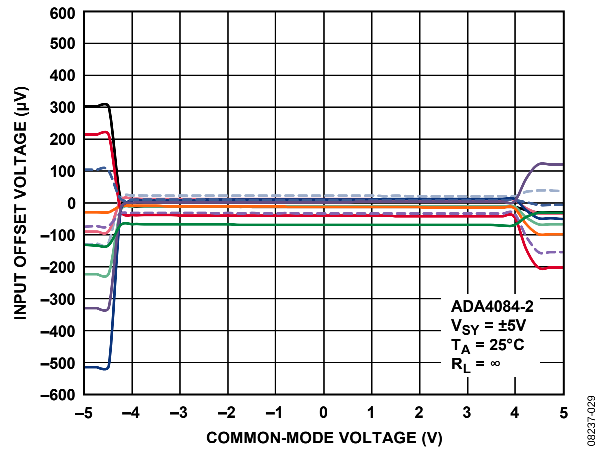

Figure 29. Input Offset Voltage vs. Common-Mode Voltage

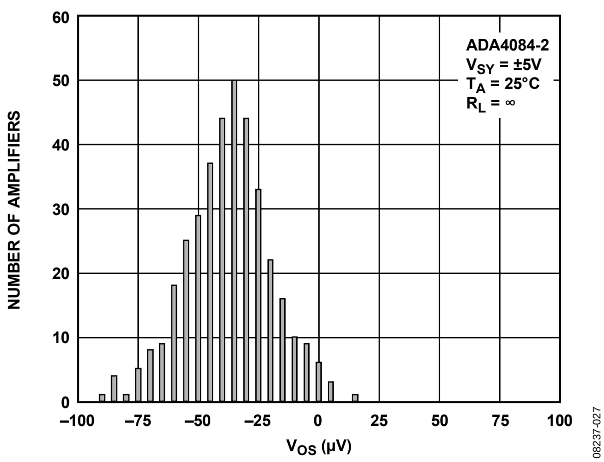

Figure 27. Input Offset Voltage Distribution MSOP

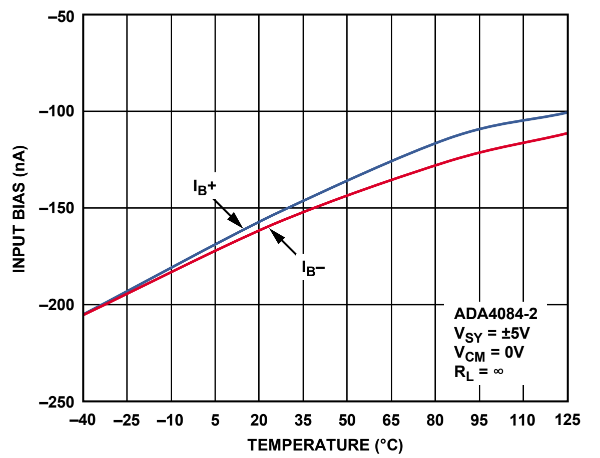

Figure 30. Input Bias Current vs. Temperature

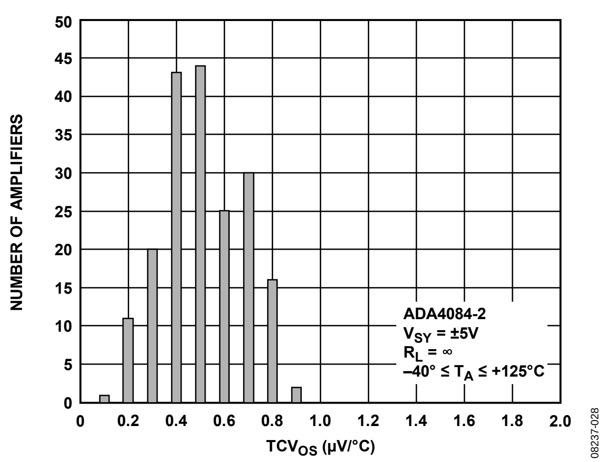

Figure 28. TCV_{OS} Distribution

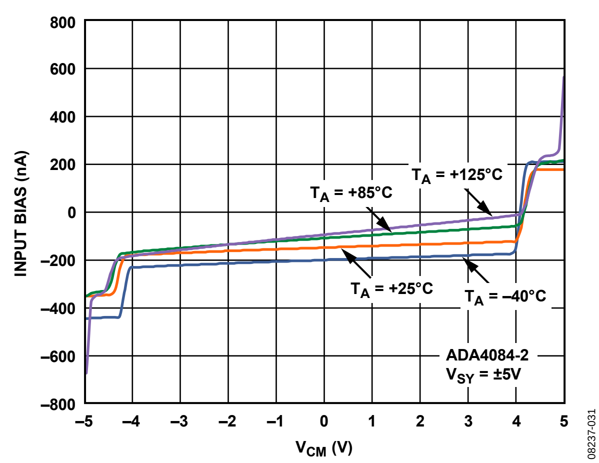

Figure 31. Input Bias Current vs. V_{CM} and Temperature

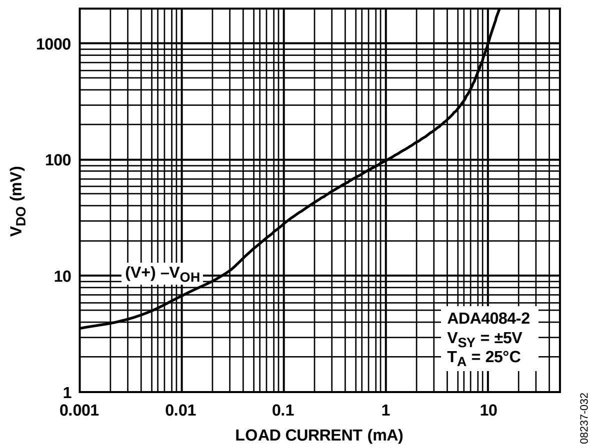

Figure 32. Dropout Voltage vs. Source Current

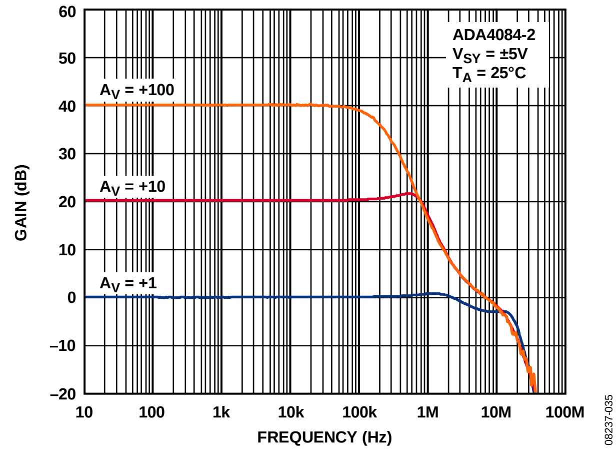

Figure 35. Closed-Loop Gain vs. Frequency

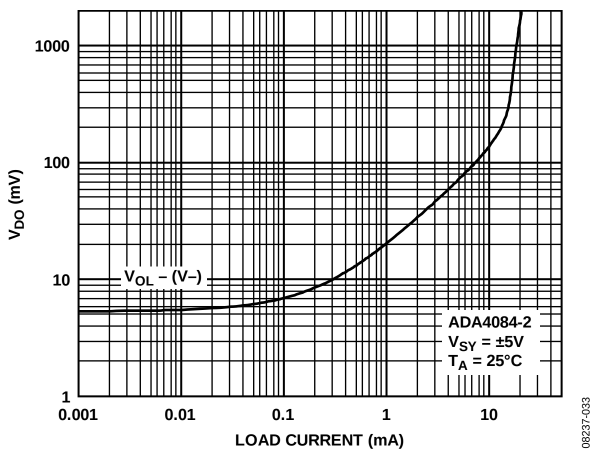

Figure 33. Dropout Voltage vs. Sink Current

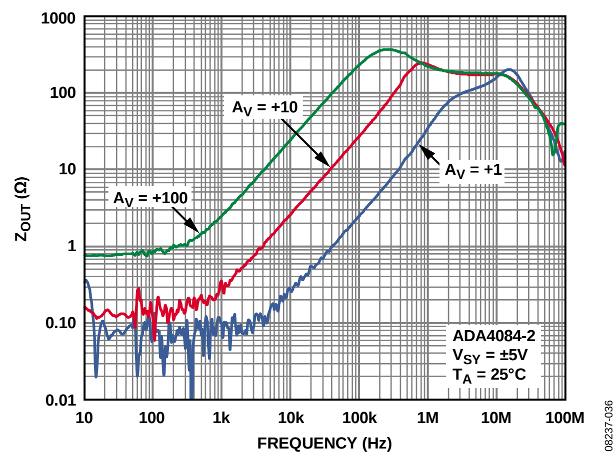

Figure 36. Output Impedance vs. Frequency

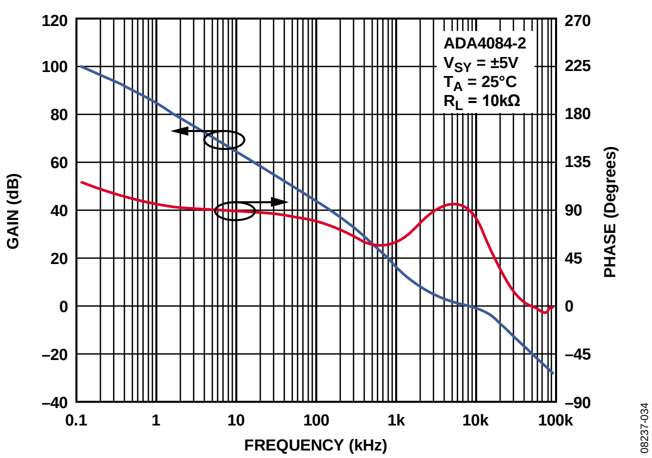

Figure 34. Open-Loop Gain and Phase vs. Frequency

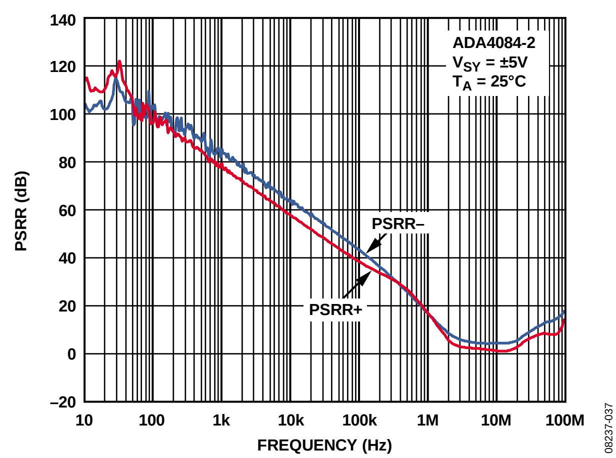

Figure 37. PSRR vs. Frequency

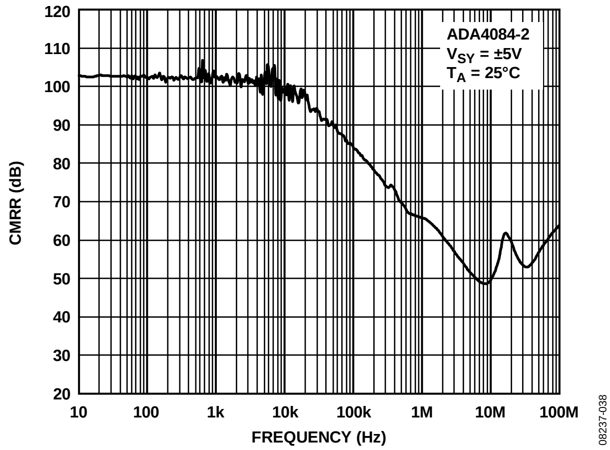

Figure 38. CMRR vs. Frequency

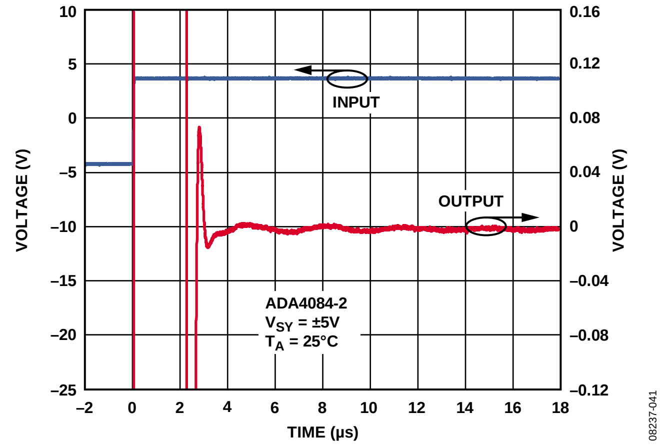

Figure 41. Settling Time

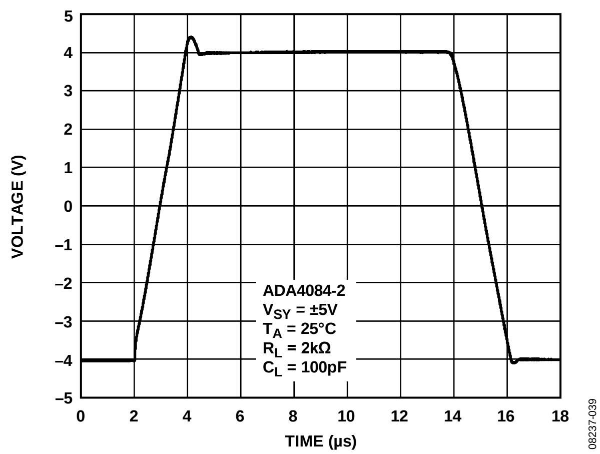

Figure 39. Large Signal Transient Response

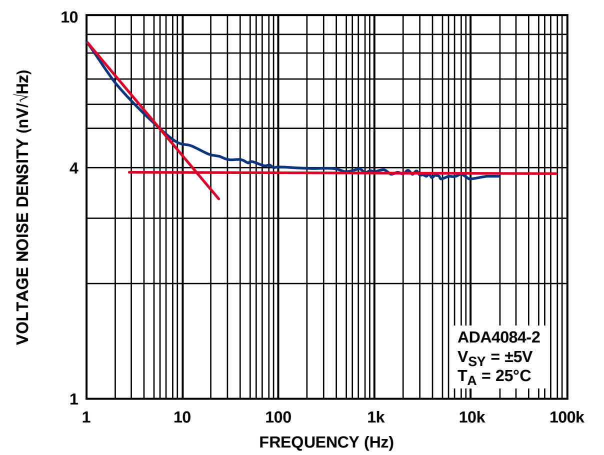

Figure 42. Voltage Noise Density

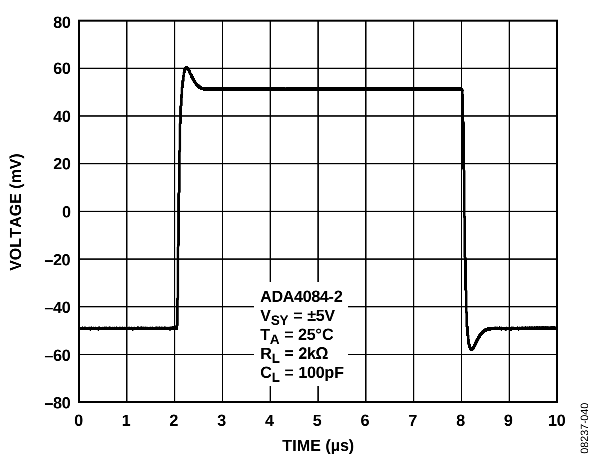

Figure 40. Small Signal Transient Response

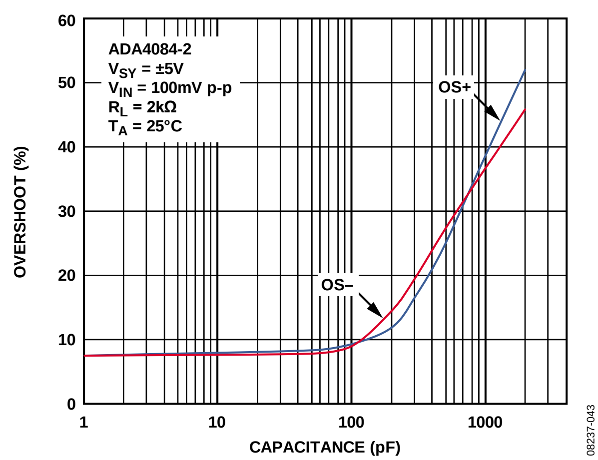

Figure 43. Overshoot vs. Load Capacitance

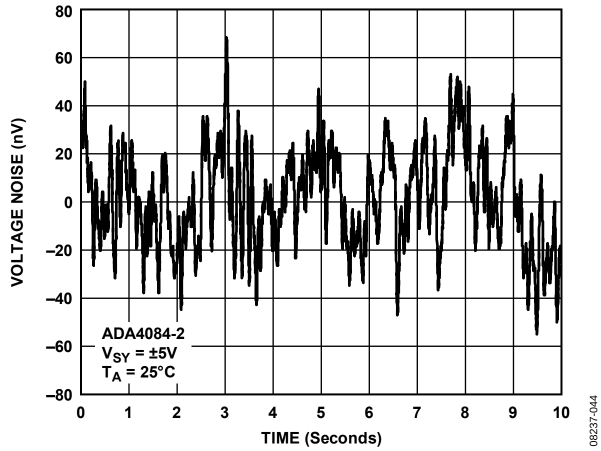

Figure 44. Volage Noise 0.1 Hz to 10 Hz

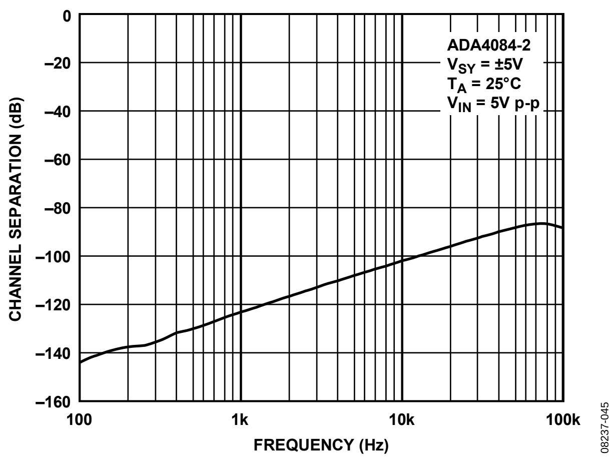

Figure 45. Channel Separation

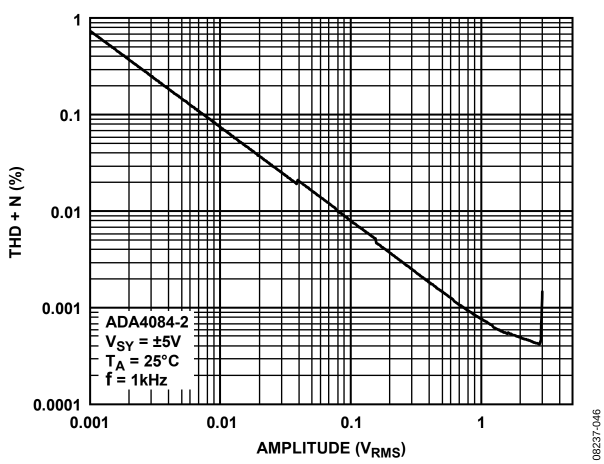

Figure 46. THD + N vs. Amplitude

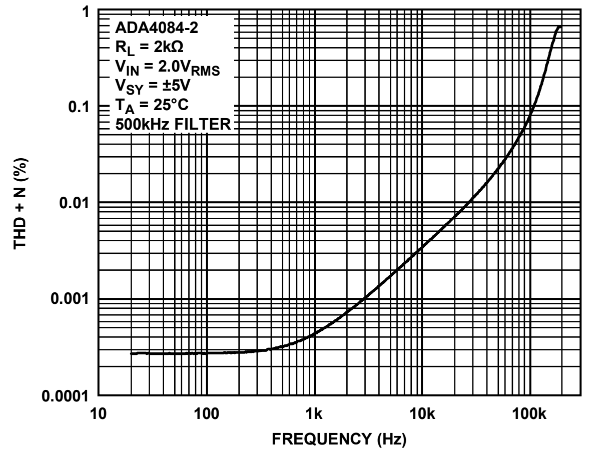

Figure 47. THD + N vs. Frequency

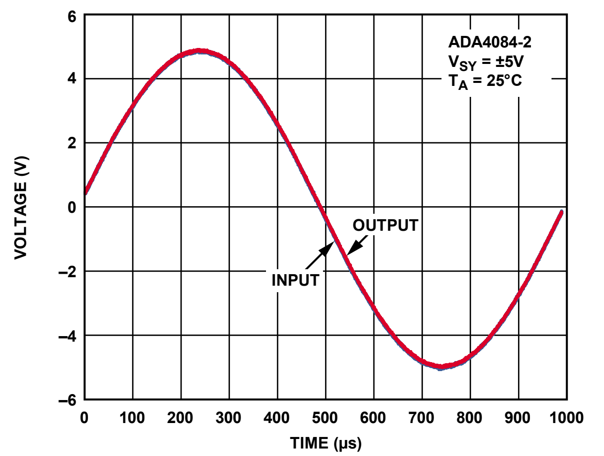

Figure 48. No Phase Reversal

±15 V CHARACTERISTICS

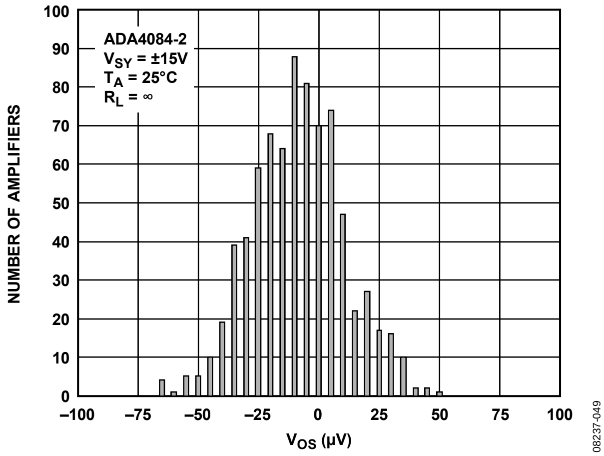

Figure 49. Input Offset Voltage Distribution, SOIC

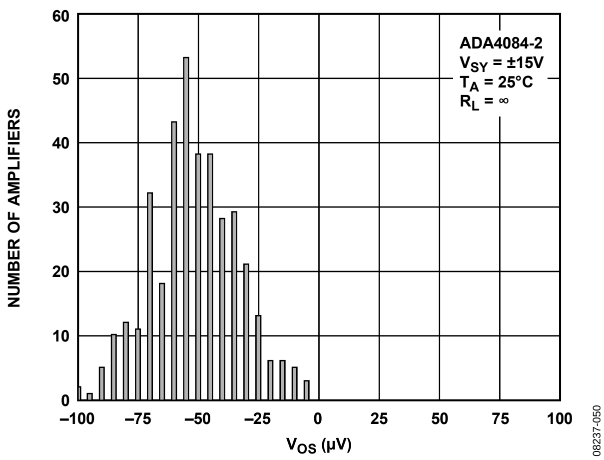

Figure 50. Input Offset Voltage Distribution, MSOP

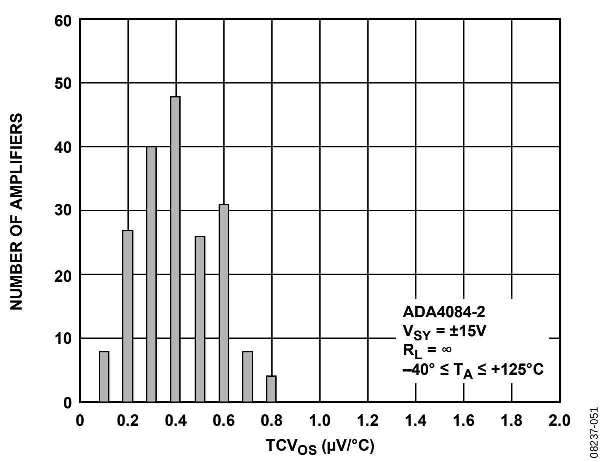

Figure 51. TCV_{OS} Distribution

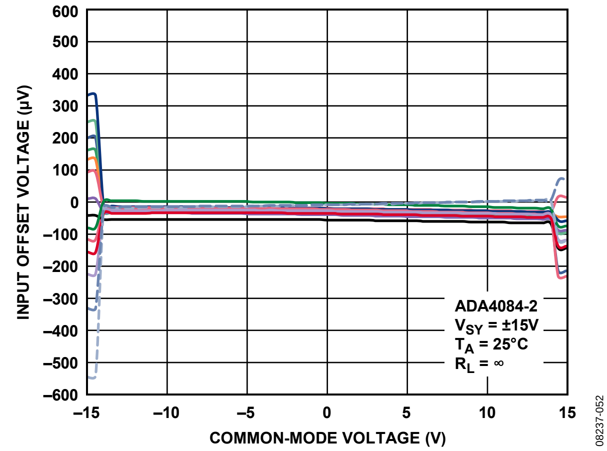

Figure 52. Input Offset Voltage vs. Common-Mode Voltage

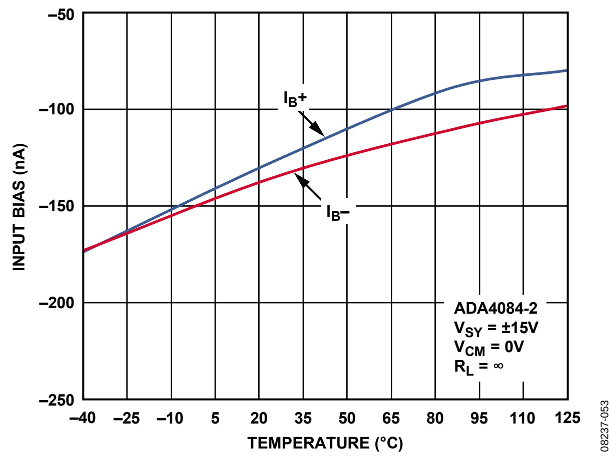

Figure 53. Input Bias Current vs. Temperature

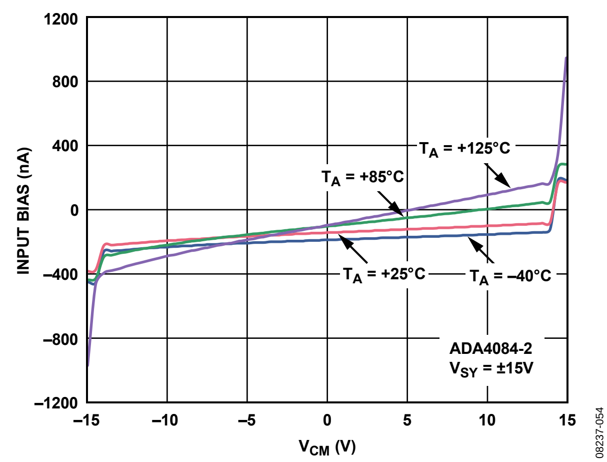

Figure 54. Input Bias Current vs. V_{CM} and Temperature

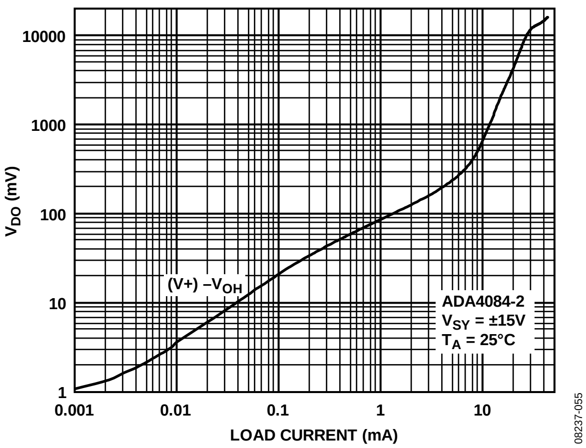

Figure 55. Dropout Voltage vs. Source Current

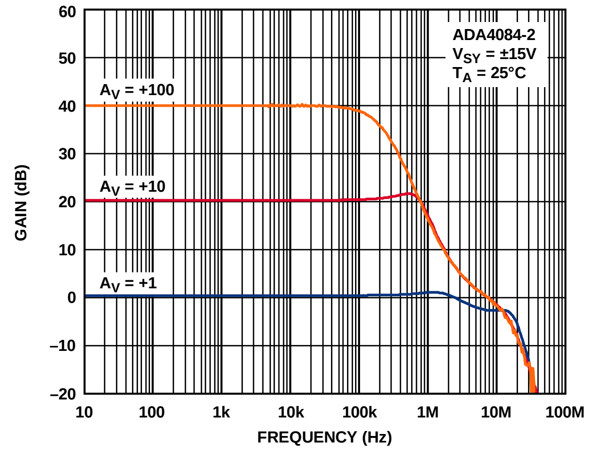

Figure 58. Closed-Loop Gain vs. Frequency

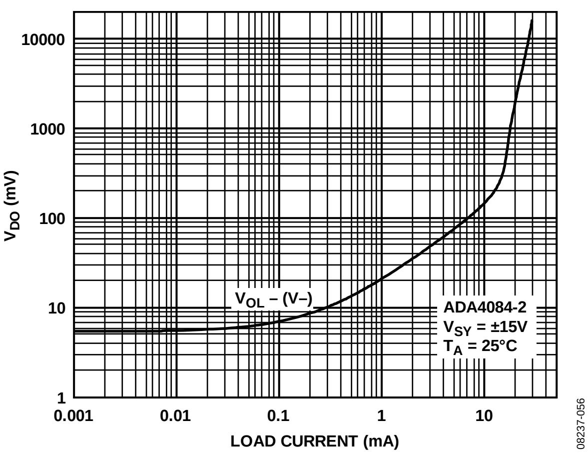

Figure 56. Dropout Voltage vs. Sink Current

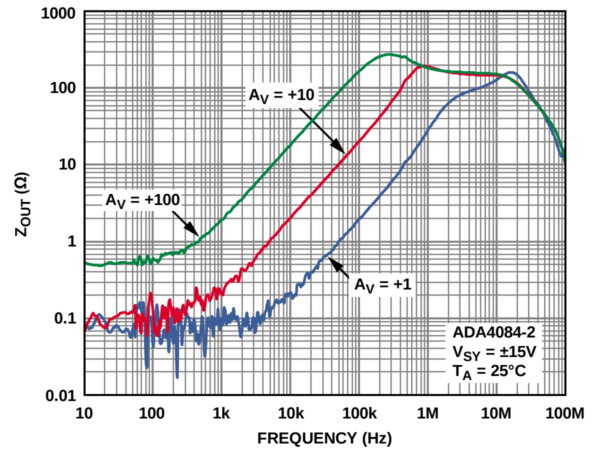

Figure 59. Output Impedance vs. Frequency

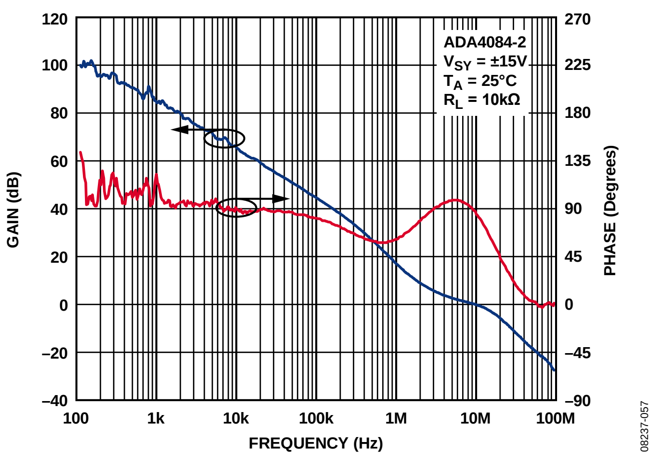

Figure 57. Open-Loop Gain and Phase vs. Frequency

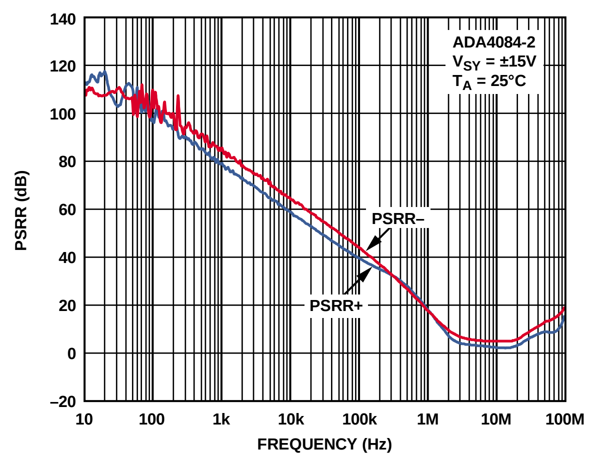

Figure 60. PSRR vs. Frequency

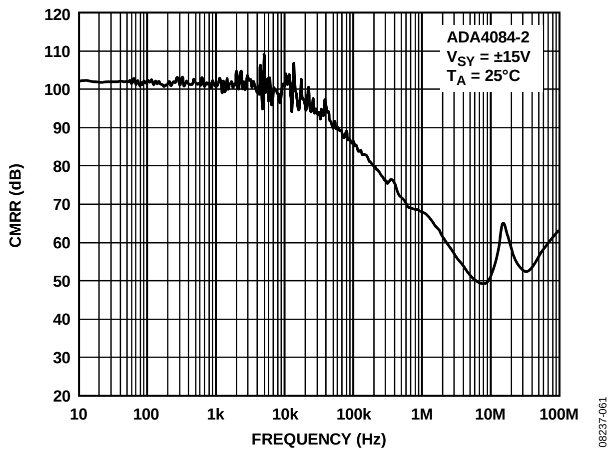

Figure 61. CMRR vs. Frequency

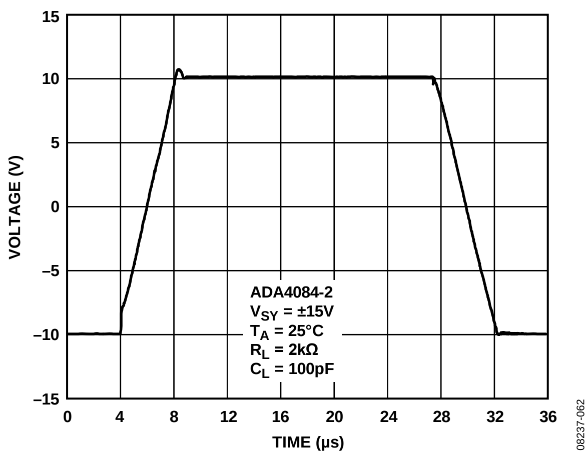

Figure 62. Large Signal Transient Response

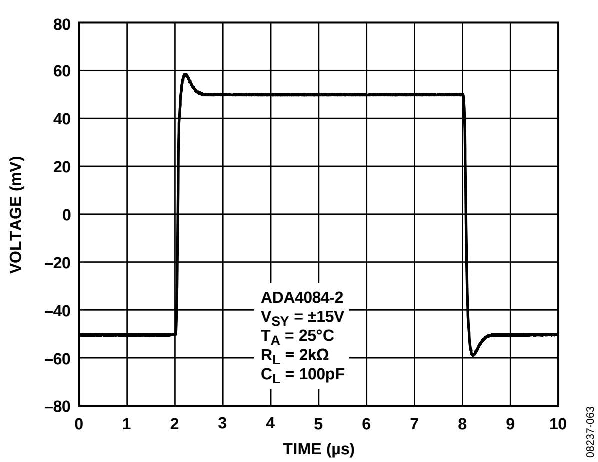

Figure 63. Small Signal Transient Response

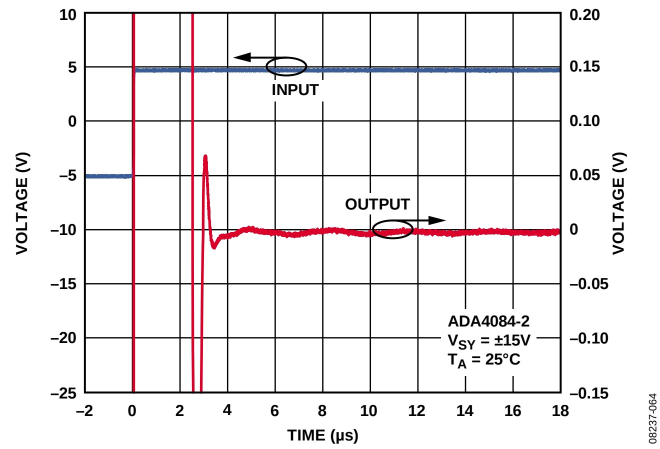

Figure 64. Settling Time

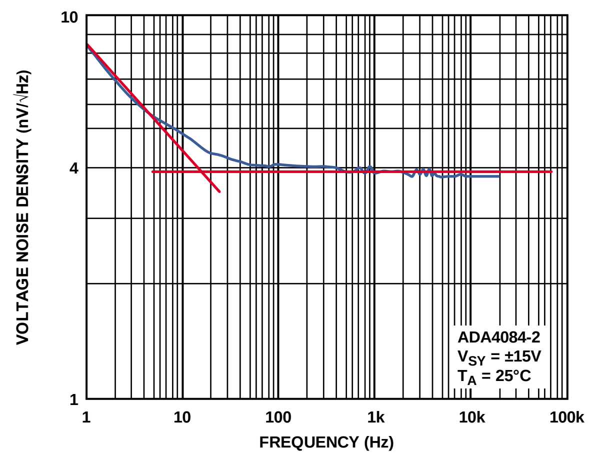

Figure 65. Voltage Noise Density

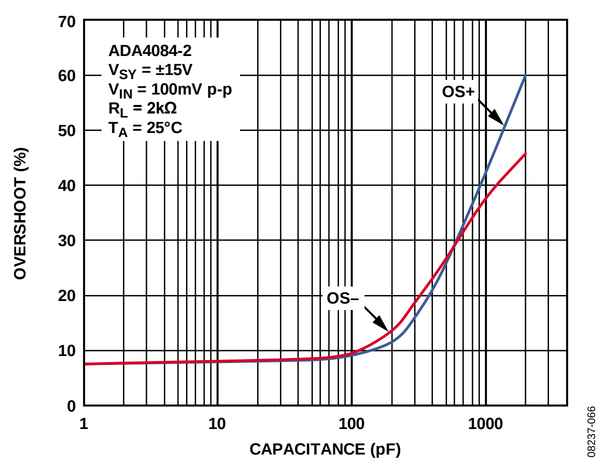

Figure 66. Overshoot vs. Load Capacitance

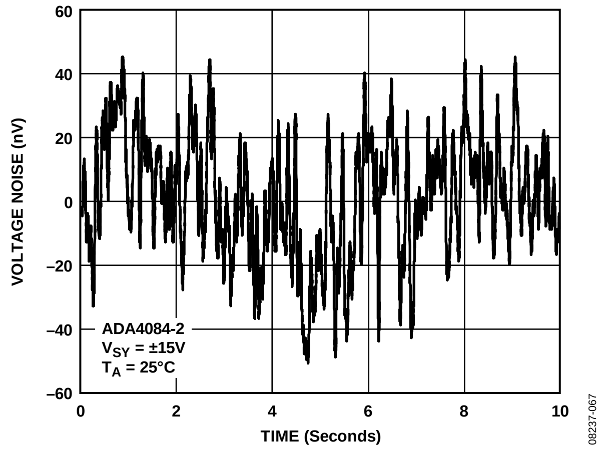

Figure 67. Voltage Noise 0.1 Hz to 10 Hz

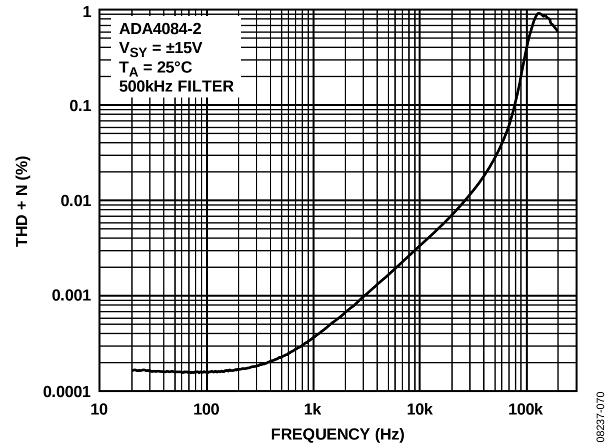

Figure 70. THD + N vs. Frequency

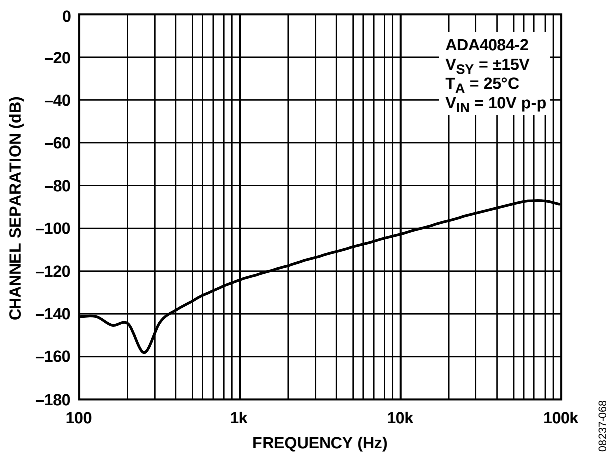

Figure 68. Channel Sepatation

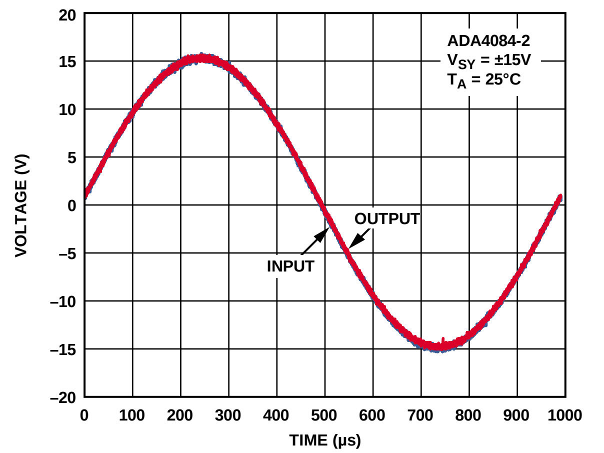

Figure 71. No Phase Reversal

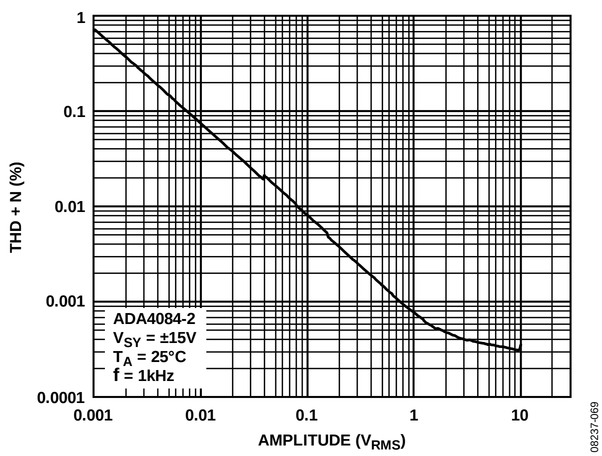

Figure 69. THD + N vs. Amplitude

COMPARATIVE VOLTAGE AND VARIABLE VOLTAGE GRAPH

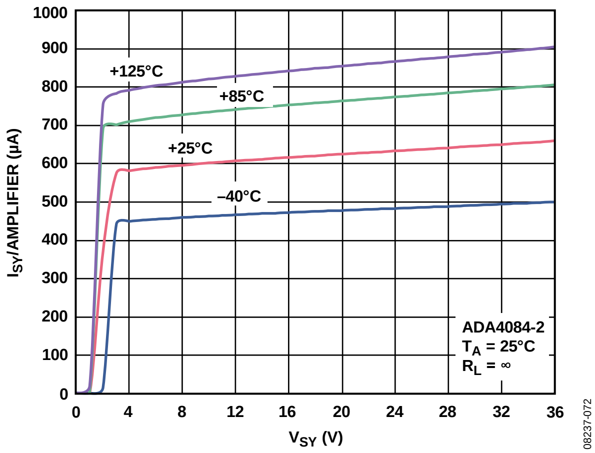

Figure 72. Supply Current vs. Supply Voltage

APPLICATIONS INFORMATION

FUNCTIONAL DESCRIPTION

The ADA4084-2 is a precision single-supply, rail-to-rail operational amplifier. Intended for portable instrumentation, the ADA4084-2 combines the attributes of precision, wide bandwidth, and low noise to make it an ideal choice in single-supply applications that require both ac and precision dc performance. Other low supply voltage applications for which the ADA4084-2 is well suited are active filters, audio microphone preamplifiers, power supply control, and telecommunications. To combine all of these attributes with rail-to-rail input/output operation, novel circuit design techniques are used.

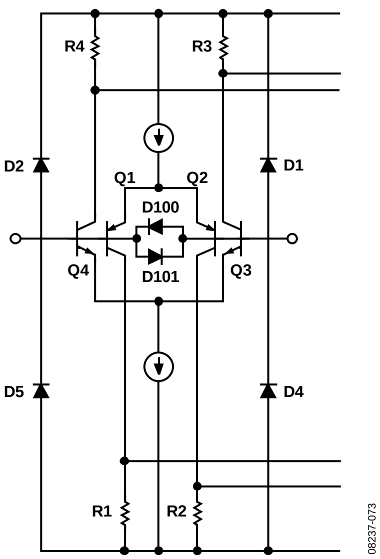

Figure 73. ADA4084-2 Equivalent Input Circuit

For example, Figure 73 illustrates a simplified equivalent circuit for the input stage of the ADA4084-2. It comprises a PNP differential pair, Q1 and Q2, and an NPN differential pair, Q3 and Q4, operating concurrently. Diode D100 and Diode D101 serve to clamp the applied differential input voltage to the ADA4084-2, thereby protecting the input transistors against Zener breakdown of the emitter-base junctions. Input stage voltage gains are kept low for input rail-to-rail operation. The two pairs of differential output voltages are connected to the second stage of the ADA4084-2, which is a modified compound folded cascade gain stage. It is also in the second gain stage, where the two pairs of differential output voltages are combined into a single-ended output signal voltage used to drive the output stage.

A key issue in the input stage is the behavior of the input bias currents over the input common-mode voltage range. Input bias currents in the ADA4084-2 are the arithmetic sum of the base currents in Q1 and Q4 and in Q2 and Q3. As a result of this design approach, the input bias currents in the ADA4084-2 not only exhibit different amplitudes; they also exhibit different polarities. This effect is best illustrated by Figure 7, Figure 8, Figure 30, Figure 31, Figure 53, and Figure 54. It is therefore important that the effective source impedances connected to the ADA4084-2 inputs be balanced for optimum dc and ac performance.

To achieve rail-to-rail output, the ADA4084-2 output stage design employs a unique topology for both sourcing and sinking current. This circuit topology is illustrated in Figure 74. The output stage is voltage-driven from the second gain stage. The signal path through the output stage is inverting; that is, for positive input signals, Q13 provides the base current drive to Q19 so that it conducts (sinks) current. For negative input signals, the signal path via Q18 → mirror → Q24 provides the base current drive for Q23 to conduct (source) current. Both transistors provide output current until they are forced into saturation.

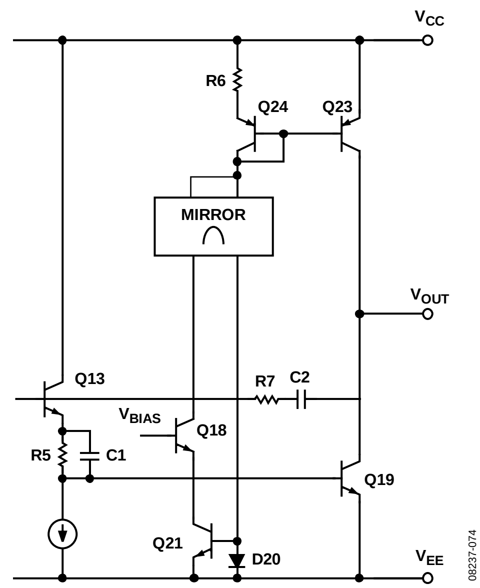

Figure 74. ADA4084-2 Equivalent Output Circuit

Thus, the saturation voltage of the output transistors sets the limit on the ADA4084-2 maximum output voltage swing. Output short-circuit current limiting is determined by the maximum signal current into the base of Q13 from the second gain stage. The output stage also exhibits voltage gain. This is accomplished by the use of common-emitter amplifiers, and, as a result, the voltage gain of the output stage (thus, the open-loop gain of the device) exhibits a dependence on the total load resistance at the output of the ADA4084-2.

INPUT PROTECTION

As with any semiconductor device, if conditions exist where the applied input voltages to the device exceed either supply voltage, the input overvoltage I-to-V characteristic of the device must be considered. When an overvoltage occurs, the amplifier may be damaged, depending on the magnitude of the applied voltage and the magnitude of the fault current.

The D1, D2, D4, and D5 diodes conduct when the input common-mode voltage exceeds either supply pin by a diode drop. This varies with temperature and is in the range of 0.3 V to 0.8 V. As illustrated in the simplified equivalent circuit shown in Figure 73, the ADA4084-2 does not have any internal current limiting resistors; thus, fault currents can quickly rise to damaging levels.

This input current is not inherently damaging to the device, provided that it is limited to 5 mA or less. If a fault condition causes more than 5 mA to flow, an external series resistor should be added at the expense of additional thermal noise. Figure 75 illustrates a typical noninverting configuration for an overvoltage-protected amplifier where the series resistance, R_S, is chosen, such that

$$R_S = \frac{V_{IN(MAX)} - V_{SUPPLY}}{5\text{ mA}}$$

For example, a 1 kΩ resistor protects the ADA4084-2 against input signals up to 5 V above and below the supplies. Note that the thermal noise of a 1 kΩ resistor at room temperature is 4 nV/√Hz, which exceeds the voltage noise of the ADA4084-2. For other configurations where both inputs are used, each input should be protected against abuse with a series resistor. Again, to ensure optimum dc and ac performance, it is recommended that source impedance levels be balanced.

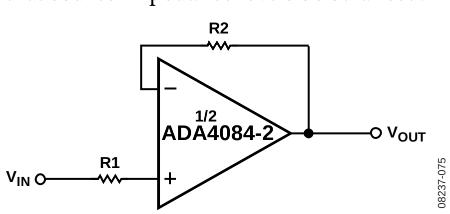

Figure 75. Resistance in Series with Input Limits Overvoltage Currents to Safe Values

To protect Q1-Q2 and Q3-Q4 from large differential voltages that may result in Zener breakdown of the emitter-base junction, D100 and D101 are connected between the two inputs. This precludes operation as a comparator. For a more complete description, see the MT-035 Tutorial, *Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues*; the MT-083 Tutorial, *Comparators*, the MT-084 Tutorial, *Using Op Amps As Comparators*; and the AN-849 Application Note, *Using Op Amps as Comparators*, at www.analog.com.

OUTPUT PHASE REVERSAL

Some operational amplifiers designed for single-supply operation exhibit an output voltage phase reversal when their inputs are driven beyond their useful common-mode range. Typically, for single-supply bipolar op amps, the negative supply determines the lower limit of their common-mode range. With these devices, external clamping diodes, with the anode connected to ground and the cathode to the inputs, prevent input signal excursions from exceeding the negative supply of the device (that is, GND), preventing a condition that causes the output voltage to change phase. JFET input amplifiers can also exhibit phase reversal, and, if so, a series input resistor is usually required to prevent it.

The ADA4084-2 is free from reasonable input voltage range restrictions, provided that input voltages no greater than the supply voltages are applied. Although device output does not change phase, large currents can flow through the input protection diodes. Therefore, the technique recommended in the Input Protection section should be applied to those applications where the likelihood of input voltages exceeding the supply voltages is high.

DESIGNING LOW NOISE CIRCUITS IN SINGLE-SUPPLY APPLICATIONS

In single-supply applications, devices like the ADA4084-2 extend the dynamic range of the application through the use of rail-to-rail operation. Referring to the op amp noise model circuit configuration illustrated in Figure 76, the expression for an amplifier's total equivalent input noise voltage for a source resistance level, R_S, is given by

$$e_{nT} = \sqrt{2\left[(e_{nR})^2 + (i_{nOA} \times R_S)^2\right] + (e_{nOA})^2}\text{, units in } \frac{\text{V}}{\sqrt{\text{Hz}}}$$

where:
$R_S = 2R$, the effective, or equivalent, circuit source resistance.
$(e_{nR})^2$ is the source resistance thermal noise voltage power (4kTR).
k is the Boltzmann's constant, 1.38×10^{-23} J/K.
T is the ambient temperature in Kelvin of the circuit, 273.15 + T_A (°C).
$(i_{nOA})^2$ is the op amp equivalent input noise current spectral power (1 Hz bandwidth).
$(e_{nOA})^2$ is the op amp equivalent input noise voltage spectral power (1 Hz bandwidth).

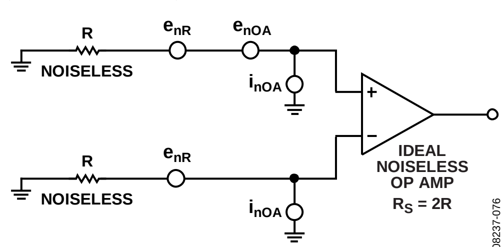

Figure 76. Op Amp Noise Circuit Model Used to Determine Total Circuit Equivalent Input Noise Voltage and Noise Figure

As a design aid, Figure 77 shows the total equivalent input noise of the ADA4084-2 and the total thermal noise of a resistor for comparison. Note that for source resistance less than 1 kΩ, the equivalent input noise voltage of the ADA4084-2 is dominant.

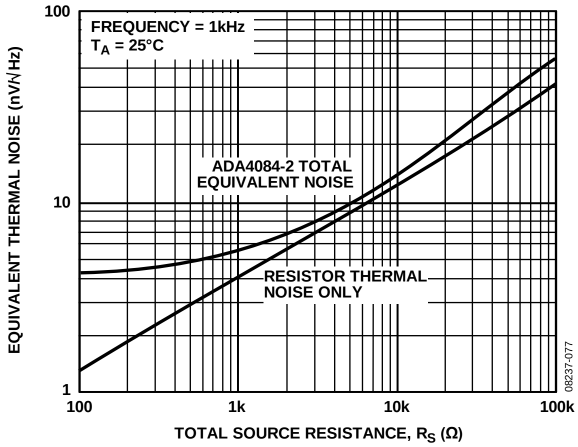

Figure 77. ADA4084-2 Equivalent Thermal Noise vs. Total Source Resistance

Because circuit SNR is the critical parameter in the final analysis, the noise behavior of a circuit is sometimes expressed in terms of its noise figure, NF. The noise figure is defined as the ratio of a circuit's output signal-to-noise to its input signal-to-noise.

Noise figure is generally used for RF and microwave circuit analysis in a 50 Ω system. This is not very useful for op amp circuits where the input and output impedances can vary greatly. For a more complete description of noise figure, see the MT-052 Tutorial, *Op Amp Noise Figure: Don't be Mislead*, available at www.analog.com.

Signal levels in the application invariably increase to maximize circuit SNR, which is not an option in low voltage, single-supply applications.

Therefore, to achieve optimum circuit SNR in single-supply applications, it is recommended that an operational amplifier with the lowest equivalent input noise voltage be chosen, along with source resistance levels that are consistent with maintaining low total circuit noise.

COMPARATOR OPERATION

Although op amps are quite different from comparators, occasionally an unused section of a dual or a quad op amp can be used as a comparator; however, this is not recommended for any rail-to-rail output op amps. For rail-to-rail output op amps, the output stage is generally a ratioed current mirror with bipolar or MOSFET transistors. With the part operating open loop, the second stage increases the current drive to the ratioed mirror to close the loop. However, it cannot, which results in an increase in supply current. With the op amp configured as a comparator, the supply current can be significantly higher (see Figure 76). An unused section should be configured as a voltage follower with the noninverting input connected to a voltage within the input voltage range. The ADA4084-2 has unique second stage and output stage designs that greatly reduce the excess supply current when the op amp is operating open loop.

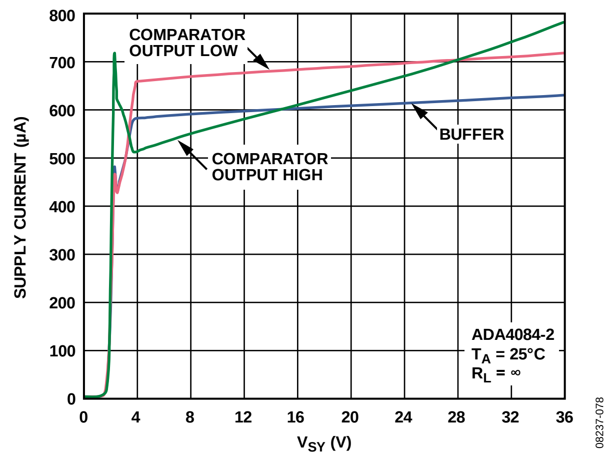

Figure 78. Supply Current vs. Supply Voltage

OUTLINE DIMENSIONS

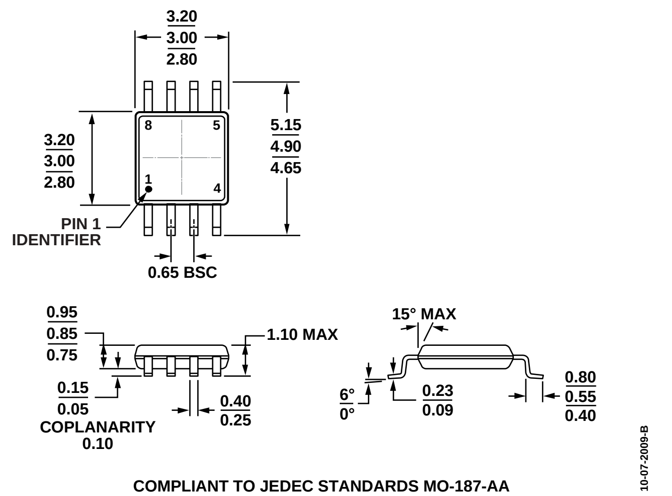

Figure 79. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

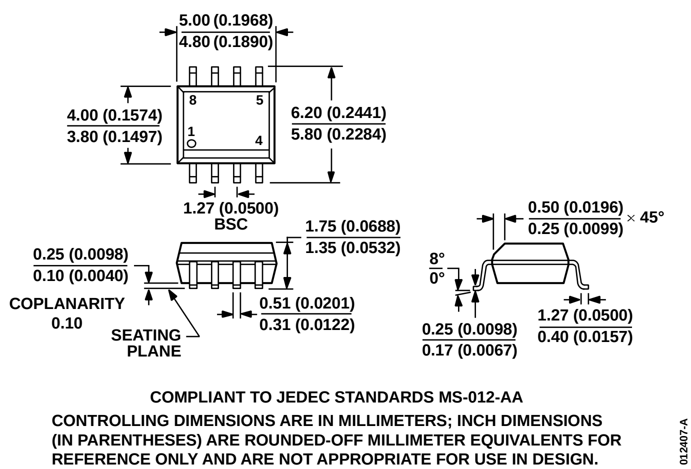

Figure 80. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADA4084-2ARMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2Q
ADA4084-2ARMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2Q
ADA4084-2ARMZ-RL	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2Q
ADA4084-2ARZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4084-2ARZ-R7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4084-2ARZ-RL	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	

[1] Z = RoHS Compliant Part.

NOTES